

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

ATTY DOCKET NO.	APPLICATION NO.
03680036AA	14587785
APPLICANT(S)	not assigned
K. Takahashi, et al.	
FILING DATE	GROUP ART UNIT
concurrently	
not assigned	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
/S.W.S./	BA	2003-258121	9/2003	Japan				✓
/S.W.S./	BB	2004-152995	5/2004	Japan				✓
/S.W.S./	BC	2004-158593	6/2004	Japan				✓

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

/S.W.S./	CA	Lee, JH, et al., "Tunable Work Function Dual Metal Gate Technology for Bulk and Non-Bulk CMOS", IEEE (2002)
/S.W.S./	CB	Kedzierski, J., et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation", IEEE (2002)

EXAMINER	/Stephen W. Smoot/	DATE CONSIDERED	08/11/2008
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INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)			ATTY DOCKET NO. 03680036AA		APPLICATION NO. 10575785 GAU: 2813			
			K. Takahashi, et al.		FILING concurrently		GROUP ART not assigned	
			U.S. PATENT DOCUMENTS					
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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
/S.W.S./	CC	Kedzierski, J., et al. "Threshold voltage control in NiSi-gated MOSFETs through silicidation induced impurity segregation (SiIS)", IEEE (2003)						
/S.W.S./	CD	Maszara, W.P., et al. "Transistors with Dual Work Function Gates by Single Full Silicidation (FUSI) of Polysilicon Gates", IEEE (2002), pp. 367-370						
EXAMINER /Stephen W. Smoot/			DATE CONSIDERED		08/11/2008			
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

/S.W.S./	CE	Terai, M., et al., "Highly Reliable HfSiON CMOSFET with Phase Controlled NiSi (NFET) and Ni3Si (PFET) FUSI Gate Electrode", Symposium on VLSI Technology Digest of Technical Papers (2005), pp. 68-69
/S.W.S./	CF	K. Takahashi, et al., "Dual Workfunction Ni-Silicide/HfSiON Gate Stacks by Phase-Controlled Full-Silicidation (PC-FUSI) Technique for 45nm-node LSTP and LOP Devices", IEEE 2004, December 2004, pp. 91-94

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